Nonlinear Parasitic Capacitance Modelling of High Voltage Power MOSFETs in Partial SOI Process

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***Abstract*—State-of-the-art power converter topologies such as resonant converters are either designed with or affected by the parasitic capacitances of the power switches. However, the power switches are conventionally characterized in terms of switching time and/or gate charge with little insight into the nonlinearities of the parasitic capacitances. This paper proposes a modelling method that can be utilized to systematically analyse the nonlinear parasitic capacitances. The existing ways of characterizing the off-state capacitance can be extended by the proposed circuit model that covers all the related states: off-state, sub-threshold region, and on-state in the linear region. A high voltage power MOSFET is designed in a partial Silicon on Insulator (SOI) process, with the bulk as a separate terminal. 3D plots and contour plots of the capacitances versus bias voltages for the transistor summarize the nonlinearities of the parasitic capacitances. The equivalent circuits in different states and the evaluation equations are provided.**

***Index Terms*—Nonlinear circuits; parasitic capacitance; power MOSFET; silicon-on-insulator.**

I. INTRODUCTION

Reductions in size, weight, and cost of power supplies are continuously being demanded by the miniaturization trend of industrial and consumer electronics [1]. The reduction of size can in principle be achieved from two perspectives: passive components and active components. Reducing the size of the passive components is related to circuit topologies with increased switching frequencies. Resonant power converters such as class DE inverters that have been developed over the years [2], [3] contribute to the size reduction of passive components, and to further reduce the size of power supplies, integrating the active components on-chip must also be considered:

First, high voltage power Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) used as main switches in power converters normally have a cellular structure composed of a mesh with parallel connected unit cells [4] to satisfy the stringent on-state resistance requirements over high temperatures and low overdriving conditions. Modern discrete power devices are constructed using a vertical channel structure where the drain and source terminals are placed on the opposite sides of a wafer, so that the distance between the two terminals can be reduced to improve the electrical performance. However, these vertical devices are not suitable for monolithic integration [4] and lateral devices where both drain and source are placed on the top side of a wafer are still the major trend for integrating the power devices with control and driver circuits on the same die. The conventional Complementary Metal–Oxide–Semiconductor (CMOS) technologies are not suitable for integrating power switches whose bulk terminals may operate at highly different voltage potentials. Silicon on Insulator (SOI) processes can take advantage of the buried oxide for dielectric isolation in vertical direction, together with the Deep Trench Isolation (DTI) and the Shallow Trench Isolation (STI) technologies for dielectric isolation in horizontal direction, so that integrating power devices at different voltage domains becomes feasible. To relax the distribution of the electric field in a pure SOI process and lead the fringing electric field to proper termination, handle wafer contacts are needed through the buried oxide for high voltage power devices. In Section II, a high voltage power MOSFET is designed as an array of parallel connected unit cells in a partial SOI process.

Second, nonlinearity analyses of the parasitic capacitances of the power MOSFETs can benefit power converter designers when investigating new topologies such as resonant power converters where the parasitic capacitances affect or participate in the operation of the resonant tank. The dynamic characteristics of power MOSFETs are often evaluated in terms of switching time and gate charge, and one of the reasons for this is the difficulties of analysing the nonlinearities of the parasitic capacitances. Industrial datasheets typically specify the input capacitance C_{iss} and the output capacitance C_{oss} with gate shorted to source [5], [6]. However, such information is very difficult to utilize and sometimes even misleading because the power MOSFETs normally operate under different conditions in real applications. Therefore, establishing a proper way to characterize the nonlinear parasitic capacitances is imperative. In Section III, a small-signal modelling method is proposed to address the nonlinearity analysis that is applicable for different transistor states: off-state, sub-threshold region, and on-state in the linear region. The detailed nonlinear parasitic capacitance analysis using the

proposed transistor model is divided into 3 sub-cases. In Section IV, the parasitic capacitances looking into the gate terminal are investigated. In Section V, the parasitic capacitances looking into the drain terminal with the transistor in off-state are investigated. In Section VI, the parasitic capacitances looking into the drain terminal with the transistor in on-state in the linear region or in the sub-threshold region are investigated. Section VII provides the conclusions of this paper.

II. A POWER MOSFET IN PARTIAL-SOI PROCESS

The high voltage power MOESFET modelled in this paper is designed in a 0.18 µm partial SOI process from X-FAB Silicon Foundries. One of the most important advantages of this process is that the SOI wafer can be combined with the deep trench isolation, forming full 3D (three-dimensional) isolation (dielectrically) between on-chip power switches.

The selected type of power MOSFET has a breakdown voltage between drain and source in excess of 110 V, a maximum operating voltage between drain and source of 100 V, a maximum operating voltage between gate and source of 5.5 V, and a minimum channel length of 0.5 µm.

The high voltage power MOSFET is designed as follows: it is composed of 96 unit cells which are connected in parallel, and each unit cell has an equivalent gate width of 100 µm, calculated as 10 fingers, each of which has a gate finger width of 10 µm. The gate length is 0.5 µm for all cells. The total of the 96 parallel connected unit cells (16 rows and 6 columns) constitutes a single, large, high voltage power MOSFET. The layout of the cell array is shown in Fig. 1. The die area is 0.2948 mm^2: the length is 692 µm and the width is 426 µm. This area includes all transistor unit cells and all deep trench isolation structures, but the associated chip pads and the electrostatic discharge (ESD) protection circuits are not shown here and are not included in the area. The silicon design has been sent to fabrication.

III. MODELLING OF POWER MOSFETs

For modelling the high voltage power MOSFETs in a partial SOI process, especially the nonlinearities of the parasitic capacitance, a small-signal modelling method is used and the proposed small-signal model of the power MOSFETs is shown in Fig. 2.

There are 4 distinct characteristics of the proposed model. First, the bulk terminal is modelled as a separate terminal. A conventional power MOSFET normally shorts the bulk terminal to the source terminal, and the corresponding gate capacitance is the sum of the gate-source capacitance and the gate-bulk capacitance.

The only way to separate the contributions of the nonlinearities of the capacitance towards bulk and source is to model the bulk as a separate terminal. Second, the proposed model includes R_{ds} as a nonlinear resistance (depending on the gate-source voltage and the drain-source voltage), both in the off-state operation and in the on-state operation, including the nonlinear behaviour in the sub-threshold region, whereas conventional modelling of power MOSFETs normally includes the nonlinear capacitances only in the off-state operation.

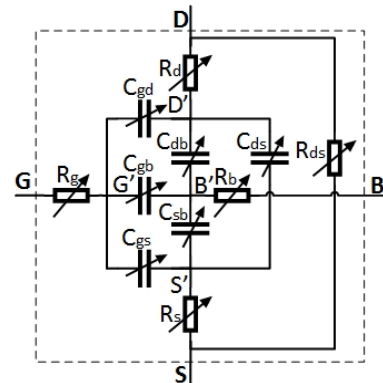Fig. 1. A high voltage power MOSFET designed in a partial SOI process.

Fig. 2. Proposed small-signal model of power MOSFETs (off-state, sub-threshold region, and on-state in the linear region).

Third, every single component in the proposed model is nonlinear (dependent on DC bias voltages). This does not only apply to the nonlinear capacitances but also apply to the nonlinear resistances. For example, the gate resistance may present nonlinear behaviour [7]. Fourth, the parasitic resistances are specifically included for drain, source, and bulk terminals. Although the values may be very small and can sometimes be neglected, in principle, the parasitic resistances always physically exist and contribute to the nonlinearities.

IV. NONLINEAR CAPACITANCES LOOKING INTO THE GATE TERMINAL

One of the key points in evaluating the nonlinearities in the modelling of power MOSFETs is to understand that the model is merely an equivalent circuit, and nonlinear capacitors in the model are not physical capacitances [8], [9], although the model may resemble the physical structures. The real transistor characteristics are much more complex than any simplified model with lumped components, and certain parts of the nonlinearities of the real transistor characteristics which do not correspond directly to the lumped components in the circuit model have to be incorporated into the descriptions of the components in the simplified equivalent model. Therefore, the resulting equivalent values of the components in the model may appear more nonlinear than the physical characteristics of a certain part of the structure. The equivalent model is used to understand and give insight into the electrical behaviour of power MOSFETs, and trying to establish a perfect match between the electrical model and the physical structures would lead to a misconception.

When all terminals of the power MOSFET are biased at fixed DC voltages, the equivalent circuit model of the

transistor shown in Fig. 2 can be further simplified in different ways, depending on which terminal of the transistor to look into, what state the transistor is in (off-state, sub-threshold region, or on-state in the linear region), and at what frequency to evaluate the model. The proposed model uses a small-signal method, and the characterization of the nonlinearities of the equivalent components uses AC signals that are superposed on certain stationary DC operating points.
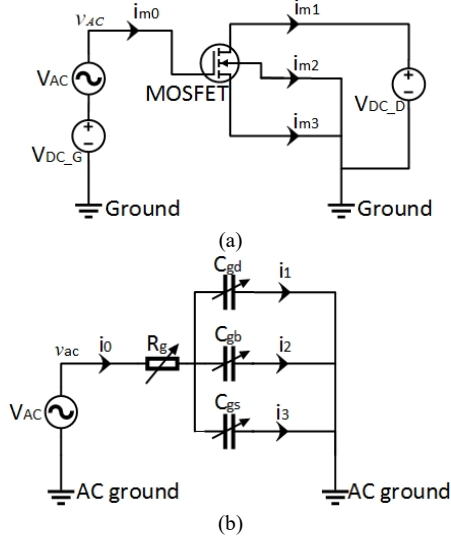

(a)

(b)

Fig. 3. Evaluation of parasitic capacitances looking into the gate terminal (off-state, sub-threshold region, and on-state in the linear region): (a) simulation setup; (b) equivalent circuit.

To evaluate the parasitic capacitance looking into the gate terminal of the power MOSFET, the simulation test bench circuit is shown in Fig. 3(a). The corresponding equivalent circuit can be derived as follows: when looking into the gate terminal of the equivalent model with drain, source, and bulk biased at fixed DC voltages, it can be assumed that the internal nodes D', S', and B' are equivalent AC ground. This is valid because R_d, R_s, and R_b in reality have very small resistance values. The assumption still holds true for physical measurements, where the external parasitic resistances and inductances from packages and interconnections do not cause practical impact. Under the conditions that the nodes D', S', and B' are equivalent AC ground, C_{db}, C_{sb}, C_{ds}, and R_{ds} can be removed from the equivalent model, and the resulting small-signal equivalent circuit is shown in Fig. 3(b). Note that each component has nonlinear values depending on the bias conditions, and that each current (and voltage) has complex values with phase component included. From Ohm's law, it is found that the equivalent nonlinear parasitic capacitance value of C_{iss} can be mathematically solved by using (1), and that C_{gd}, C_{gb}, and C_{gs} can afterwards be determined by using (2)–(4).

In (1), the imaginary part of the impedance is taken into account for calculating the capacitance value of C_{iss}, because as the input frequency f_s increases, the magnitude of the imaginary part of the impedance decreases, so that the magnitude of the resistive part of the impedance becomes comparable to the magnitude of the imaginary part of the impedance. Therefore, estimating the capacitance values using the total impedance would lead to huge errors or even wrong results at high frequencies:

$$c_{iss} = c_{gd} + c_{gb} + c_{gs} = \frac{1}{2\pi \times f_s \times \left| \text{Im}\left(v_{ac}/i_0 \right) \right|}, \quad (1)$$

$$c_{gd} \cong \frac{|i_1|}{|i_0|} \times c_{iss}, \quad (2)$$

$$c_{gb} \cong \frac{|i_2|}{|i_0|} \times c_{iss}, \quad (3)$$

$$c_{gs} \cong \frac{|i_3|}{|i_0|} \times c_{iss}. \quad (4)$$

For evaluating the nonlinear parasitic capacitance, an input frequency f_s of 1 MHz is used, as it is the industrial standard measurement frequency [5], [6]. At higher frequencies, the equivalent series resistance associated with the physical capacitive structures may influence the results. Since it is a distributed capacitive structure, it is a non-trivial task to include the physically distributed parasitic resistance in the transistor model (e.g. as equivalent series resistances to C_{gd}, C_{gb}, and C_{gs}). Using a model with a lumped capacitor C_{iss}, the distributed physical nature of the structure may cause the equivalent lumped capacitor value of C_{iss} to show a decrease with increasing frequency. Simultaneously, the equivalent lumped capacitor values of C_{gd}, C_{gb}, and C_{gs} may show either an increase or a decrease, depending on the unbalance of the distributed parasitic resistances of the drain, bulk, and source.

The simulation results of the equivalent nonlinear parasitic capacitances when looking into the gate terminal are shown in Fig. 4 for $V_D = V_B = V_S = 0$ V. The simulations are based on the HiSIM-HV models [10] for the SOI process used for fabricating the chip.

From the simulation results in Fig. 4, it is worth noting that the equivalent capacitance C_{iss} is dominated by different sub-capacitances in 3 regions: when the fixed DC bias voltage at the gate terminal V_G is negative, C_{iss} is mainly dominated by the gate-bulk capacitance C_{gb}; when V_G is near 0 V, implying that the gate and source bias voltages are close to each other, C_{iss} is mainly dominated by the gate-drain capacitance C_{gd}; when V_G is larger than the threshold voltage of the power MOSFET ($V_{th} \approx 1.1$ V), C_{iss} is mainly dominated by the gate-source capacitance C_{gs}.

The gate input capacitance C_{iss} (when bulk shorts to source) does not originate solely from the gate-source capacitance C_{gs} (and the gate-drain capacitance C_{gd}). Ignoring the gate-bulk capacitance C_{gb} would give huge errors at negative gate voltages, though at positive gate voltages, the difference may be rather small.

The nonlinear behaviour of the equivalent capacitance C_{iss} looking into the gate terminal is shown in Fig. 5 with different combinations of the gate voltage (0 V–5 V) and the drain voltage (0 V–5 V). This covers all the transistor states that power switches normally work in, i.e. the off-state, the sub-threshold region, and the on-state in the linear region.

The curve at the edge for $V_D = 0$ V and $V_G = 0$-5 V in Fig. 5(a) shows the same curve of C_{iss} for the same voltage range as shown in the right part of Fig. 4. (Note that the x-axes are different). The curve at the edge for $V_G = 0$ V and $V_D = 0$-5 V shows a monotonically decreasing function from 28.83 pF to 11.25 pF. The curve at the edge for $V_G = 5$ V and $V_D = 0$-5

V shows a monotonically increasing function from 53.82 pF to 55.16 pF with very small derivatives. From the 3D plot in Fig. 5(a), it is clear that extrapolating the nonlinear C_{iss} values based solely on a 2D plot at a certain drain or gate voltage would be inappropriate, because the nonlinear C_{iss} can either increase or decrease at different drain or gate voltages. From the contour plot in Fig. 5(b), it can be observed that at a fixed drain voltage, as the gate voltage increases, the nonlinear capacitance C_{iss} has either a large range of small capacitance values at the foot of a narrow and big mountain (high V_D), or a smaller range of small capacitance values at the foot of a wide and small hill (small V_D).
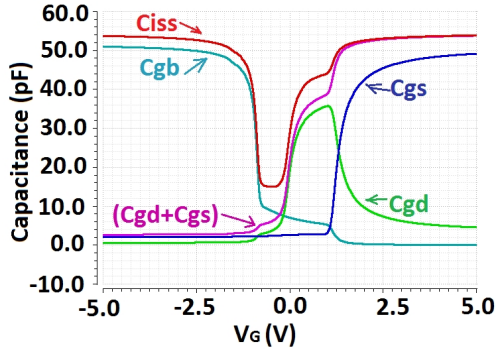
Fig. 4. Nonlinear parasitic capacitances looking into the gate terminal ($V_D = V_B = V_S = 0$ V).
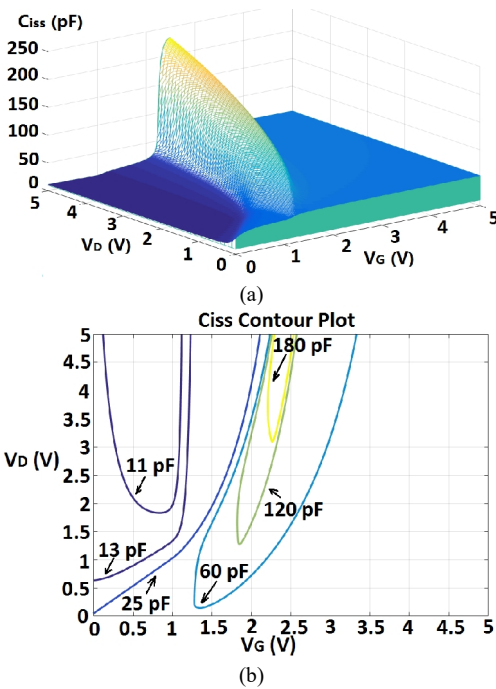

(a)

(b)

Fig. 5. Nonlinearities of C_{iss} (off-state, sub-threshold region, and on-state in the linear region, $V_B = V_S = 0$ V): (a) C_{iss} in 3D plot; (b) C_{iss} in contour plot.

In the simplified equivalent circuit in Fig. 3(b), it has been assumed that R_d in the small-signal model of power MOSFETs (in Fig. 2) has a very small resistance value and can be removed from the model when looking into the gate terminal. To evaluate the actual impact of R_d, an effective way is to add an external series resistance to the drain terminal and then determine the equivalent capacitances using the same modelling method. The simulation results of the equivalent capacitances versus the external series resistance value at the drain terminal are shown in Fig. 6(a).
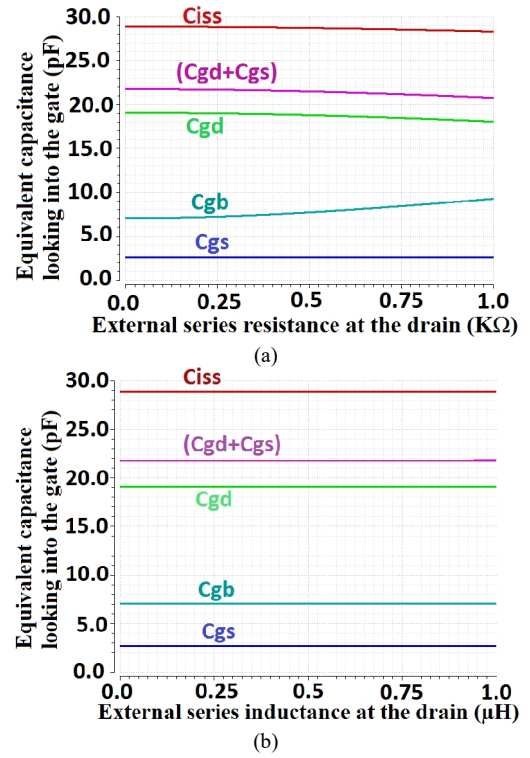

(a)

(b)

Fig. 6. Equivalent capacitances looking into the gate with external series resistance or inductance at the drain ($V_G = V_D = V_B = V_S = 0$ V): (a) external series resistance at the drain; (b) external series inductance at the drain.

All the equivalent capacitances change very little with increasing external resistance, and the gate-bulk capacitance C_{gb} is most affected. When the external resistance is about 360 Ω, C_{gb} increases by 5 %. When the external resistance increases from 0 KΩ to 1 KΩ, C_{gb} increases by 31.07 % from 7.08 pF to 9.28 pF. Similarly, an external series inductance can be added to the drain terminal, leading to the simulation results shown in Fig. 6(b). When the external inductance increases from 0 µH to 1 µH, the equivalent capacitances almost do not change (< 0.4 %). Therefore, it can be concluded that even the simplified circuit model works very well in practical conditions.

V. NONLINEAR CAPACITANCES LOOKING INTO THE DRAIN TERMINAL AT OFF-STATE

To determine the corresponding equivalent nonlinear parasitic capacitances, the situation is different when looking into the drain terminal, compared to looking into the gate terminal. This is because there is a direct resistive path from the drain terminal towards AC ground through the nonlinear resistance R_{ds}. The situation is divided into two sub-cases: 1) when the transistor is in off-state and the gate voltage is much lower than the threshold voltage, and 2) when transistor is in on-state in the linear region or in the sub-threshold region.

For the first case, R_{ds} between the drain terminal and the source terminal has an equivalent resistance in the MΩ to GΩ range, implying that R_{ds} can be removed from the equivalent model. In this case, the situation is very similar to the situation in the previous section. To evaluate the parasitic capacitances looking into the drain terminal, the simulation test bench circuit is shown in Fig. 7(a). The corresponding equivalent circuit can be derived as follows: when looking into the drain terminal of the equivalent model with the gate, bulk, and

source terminals biased at fixed DC voltages, the internal nodes G', B', and S' can be assumed to be equivalent AC ground. Then C_{gb}, C_{gs}, and C_{sb} can be removed from the equivalent model, and the resulting small-signal equivalent circuit is shown in Fig. 7(b).
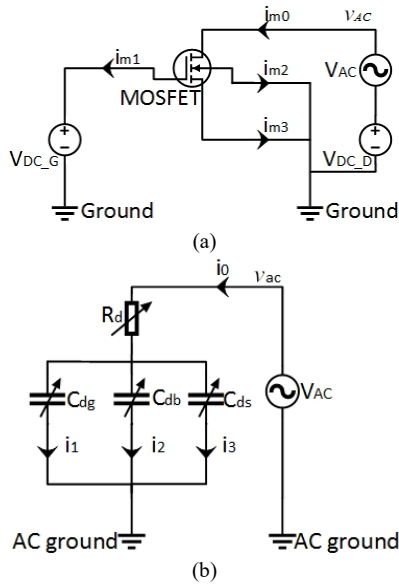

(a)

(b)

Fig. 7. Evaluation of parasitic capacitances looking into the drain terminal (off-state): (a) simulation setup; (b) equivalent circuit.

The corresponding nonlinear parasitic capacitance values can be determined by the following equations (5)–(8):

$$c_{oss} = c_{dg} + c_{db} + c_{ds} = \frac{1}{2\pi \times f_s \times \left| \text{Im}\left(v_{ac} / i_0 \right) \right|}, \quad (5)$$

$$c_{dg} \cong \frac{|i_1|}{|i_0|} \times c_{oss}, \quad (6)$$

$$c_{db} \cong \frac{|i_2|}{|i_0|} \times c_{oss}, \quad (7)$$

$$c_{ds} \cong \frac{|i_3|}{|i_0|} \times c_{oss}. \quad (8)$$

The simulation results of the equivalent nonlinear parasitic capacitance when looking into the drain terminal are shown in Fig. 8 for $V_G = V_B = V_S = 0$ V. The equivalent capacitance C_{oss} is mainly dominated by the drain-bulk capacitance C_{db}. The drain-source capacitance C_{ds} shows very small values, because the transistor is biased in off-state with the gate voltage of 0 V, and there is no channel for majority carries formed in the lateral device: in a partial SOI process, the drain diffusion and the source diffusion are separated far apart.

Therefore, the situation is very different from the situation that there is a direct and large junction between the P-body and N⁻ epitaxial layer in conventional vertical devices [11].

The nonlinear behaviour of the equivalent capacitance C_{oss} looking into the drain terminal is shown in Fig. 9 with different combinations of the gate voltage (0 mV–700 mV) and the drain voltage (0 V–5 V). Note that in these voltage ranges, the transistor is in off-state and the gate voltage is much lower than the threshold voltage ($V_{th} \approx 1.1$ V). The curve at the edge for $V_G = 0$ V and $V_D = 0$-5 V in Fig. 9(a)

shows the same curve of C_{oss} for the same voltage range as shown in the left part of Fig. 8. The curve at the edge for $V_D = 0$ V and $V_G = 0$-700 mV shows a monotonically increasing function from 55.10 pF to 70.54 pF. The curve at the edge for $V_D = 5$ V and $V_G = 0$-700 mV shows a monotonically increasing function from 6.072 pF to 6.140 pF with very small derivatives. This phenomenon can be observed from the contour plot of C_{oss} in Fig. 9(b) as well.
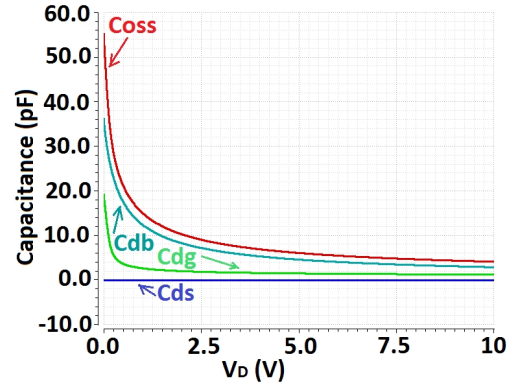

Fig. 8. Nonlinear parasitic capacitances looking into the drain terminal (off-state, $V_G = V_B = V_S = 0$ V).
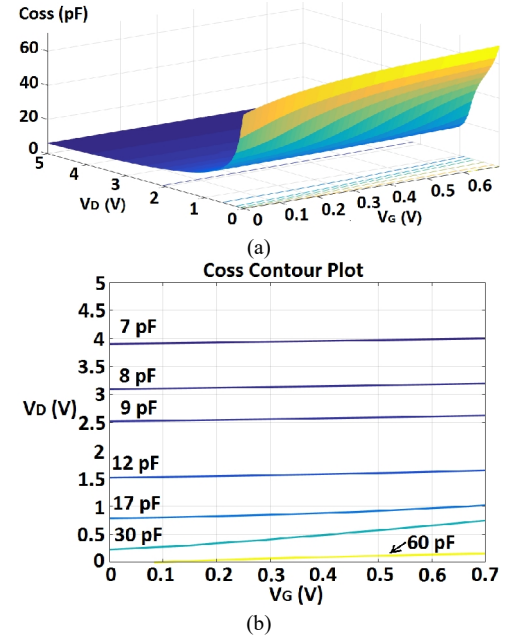

(a)

(b)

Fig. 9. Nonlinearities of C_{oss} (off-state and the gate voltage is much lower than the threshold voltage, $V_B = V_S = 0$ V): (a) C_{oss} in 3D plot; (b) C_{oss} in contour plot.

It may be noticed that R_g has been removed from the simplified equivalent circuit in Fig. 7(b) to determine the nonlinear parasitic capacitances when looking into the drain terminal. This corresponds to the industrial standard way [12] of measuring C_{oss} by directly shorting the gate terminal to the source terminal, and then measuring or calculating the equivalent capacitance between the drain terminal and AC ground [7], [12]. This is equivalent to omitting R_g from the measurement circuit.

To evaluate the actual impact of R_g, an effective way is to add an external series resistance to the gate terminal and then determine the equivalent capacitances using the same modelling method. The simulation results of this evaluation are shown in Fig. 10(a). The equivalent capacitances almost

do not change (< 0.6 %) with increasing external resistance, except for the drain-gate capacitance C_{dg}. When the external resistance increases from 0 KΩ to 1 KΩ, C_{dg} looking into the drain terminal decreases by 1.52% from 19.06 pF to 18.77 pF. Again, an external series inductance can be added to the gate terminal, leading to the simulation results shown in Fig. 10(b).
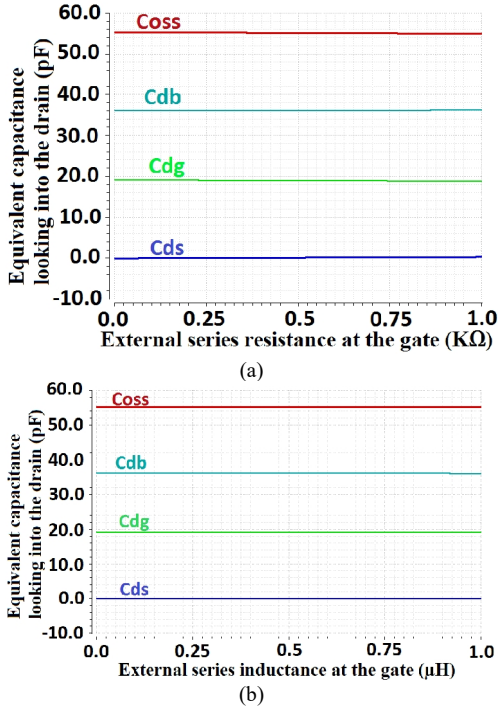

(a)

(b)

Fig. 10. Equivalent capacitances looking into the drain with external series resistance or inductance at the gate ($V_G = V_D = V_B = V_S = 0$ V): (a) external series resistance at the gate; (b) external series inductance at the gate.
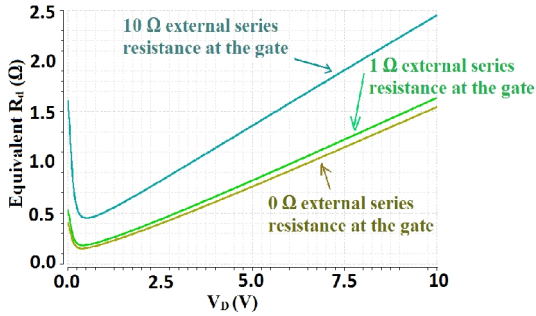

Fig. 11. Equivalent R_d looking into the drain with different external series resistance at the gate ($V_G = V_B = V_S = 0$ V).

When the external inductance increases from 0 µH to 1 µH, the equivalent capacitances almost do not change (< 0.2 %). Therefore, it can be concluded that the simplified circuit model also works very well in practical conditions, when evaluating the nonlinear parasitic capacitances looking into the drain terminal.

The nonlinear equivalent resistance R_d that is determined using the equivalent circuit in Fig. 7(b) when looking into the drain terminal is shown in Fig. 11. It shows that the external series resistance at the gate indeed contributes to the nonlinearities of the equivalent resistance R_d, and this is because R_d as the only resistive component in the simplified equivalent circuit has to model all the effects resulting from a finite value of the total resistance at the gate.

VI. NONLINEAR CAPACITANCES LOOKING INTO THE DRAIN TERMINAL IN ON-STATE IN THE LINEAR REGION OR IN THE SUB-THRESHOLD REGION

As discussed in the previous section, the second sub-case is when the transistor is in on-state in the linear region or in the sub-threshold region. The simulation test bench circuit is the same one as shown in Fig. 7(a). For the sub-threshold region, the equivalent resistance R_{ds} is in the KΩ range or even lower, so it cannot be neglected compared to the impedance of the parasitic capacitances. The equivalent circuit can be derived from Fig. 7(b) by adding R_{ds} directly between the drain and the source terminals. The resulting equivalent circuit is shown in Fig. 12, where the dotted box denotes the transistor boundary.
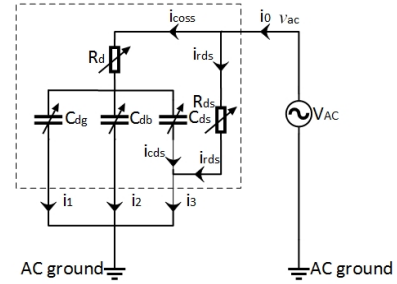

Fig. 12. Equivalent circuit looking into the Drain terminal (on-state in the linear region or in the sub-threshold region).
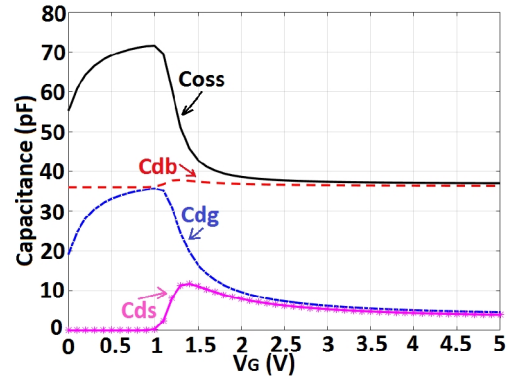

Fig. 13. Nonlinear parasitic capacitances looking into the drain terminal (on-state in the linear region or in the sub-threshold region, as well as off-state, $V_D = 1$ µV, $V_B = V_S = 0$ V).

The nonlinear resistance R_{ds} can be measured at DC using a small DC bias voltage for the drain voltage. With the value of R_{ds} in place, the nonlinear parasitic capacitance values can be estimated by the following equations (9)–(13) (recall that each AC current has its phase included, and the minus sign is not simple subtraction of magnitudes):

$$i_{rds} \approx \frac{v_{ac}}{R_{ds}}, \qquad (9)$$

$$c_{oss} = c_{dg} + c_{db} + c_{ds} = \frac{1}{2\pi \times f_s \times \left| \mathrm{Im}\left(v_{ac} / \left(i_0 - i_{rds} \right) \right) \right|}, \qquad (10)$$

$$c_{dg} \cong \frac{|i_1|}{|i_0 - i_{rds}|} \times c_{oss}, \qquad (11)$$

$$c_{db} \cong \frac{|i_2|}{|i_0 - i_{rds}|} \times c_{oss}, \qquad (12)$$

$$c_{ds} \cong \frac{|i_3 - i_{rds}|}{|i_0 - i_{rds}|} \times c_{oss}. \qquad (13)$$

Finally, the nonlinear parasitic capacitances looking into the drain terminal are shown in Fig. 13 for the case when the transistor is in on-state in the linear region or in the sub-threshold region. The equivalent circuit for these conditions works for the off-state as well, and the part of the C_{oss} curve for $V_G = 0\text{-}700$ mV in Fig. 13 matches exactly with the C_{oss} curve for the same voltage range in Fig. 9(a), even though the results are achieved using different equivalent circuits with and without R_{ds}. Note that the drain voltage has a DC bias value of 1 μV because the nonlinear resistance R_{ds} must be found for the bias point used for the AC simulations, and the drain voltage has to be kept as small as possible to avoid the nonlinear effects at higher drain voltages. The nonlinearities are not analyzed at the high drain voltages when the transistor is switched on, because power switches do not normally operate with a high drain voltage in on-state as this causes large losses. C_{oss} in off-state and in the sub-threshold region is dominated by the parasitic capacitances C_{db} and C_{dg} together, and C_{oss} in on-state in the linear region is mainly dominated by C_{db}. The parasitic capacitance C_{ds} has its peak value when the gate voltage is slightly above the threshold voltage.

VII. CONCLUSIONS

A high voltage power MOSFET with a drain to source breakdown voltage above 100 V is designed in a 0.18 μm partial SOI process. It is composed of 96 parallel connected unit cells with a gate length of 0.5 μm, and the die area is 0.2948 mm^2 for the transistor array.

The power MOSFET is modeled using a small-signal modeling method, with the bulk as a separate terminal. The proposed circuit model is applicable for all the relevant transistor states: off-state, sub-threshold region, and on-state in the linear region. The nonlinearity analysis is divided into 3 sub-cases, which are analyzed separately. The input capacitance C_{iss} and the output capacitance C_{oss} are separated into sub-components, and it is found that the parasitic capacitances towards the bulk can dominate over the parasitic capacitances towards the source in this lateral device. The 3D plots and the contour plots reveal the overall nonlinear dependencies of the parasitic capacitances on the bias voltages.

FUTURE WORK

The switching behavior and the temperature behavior of the proposed small-signal model can be further investigated as future work. The theoretical behavior might be derived in one of the following ways: 1) calculate a linear formula or do a two-dimensional numerical simulation of the cell structure [13], 2) use a piecewise linear model or solve a derivatives matrix [10], or 3) apply semiconductor physics in different device regions (*e.g.* accumulation, depletion, weak inversion, moderate inversion, strong inversion saturation, and strong inversion non-saturation) [14].

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